REMARKS

Claims 6, 7, 15-17, 19-22, 24 and 68 are pending in the application, and rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. However, the Examiner does state that the claims contain allowable subject matter.

Applicant has amended to claims to address the rejections as discussed below.

Claim 6: The Examiner asserts that the limitation "a pull-up and/or pull-down circuit in which the second power source is supplied with to a level conversion output of a level conversion core circuit" is unclear. Applicant has amended the claim such that it indicates that the pull-up and/or pull-down is connected to the output of the level conversion core circuit.

Next, the Examiner argues that the limitation "the third logic circuit generating a control signal under control of the first power source (VDDL)" is misdescriptive. Applicant disagrees; however, claim 6 has been further clarified. Also, Applicant notes that the second power source (VDDH) is simply a power source to the third logic circuit. The specification explains that the third logic circuit is under the control of the first power source (VDDL). See for example, figure 28 and pages 46 and 47. The specification explains that E0, E1 and E2 are controlled based on the state change of VDDL such that the control signals are change to low before turning the first power source to off, and the control signals are changed to high after turning the first power source to on.

Claim 7: Applicant has amended claim 7 to clarify that the control signal is the second control signal in claim 6.

Claims 17, 21, 22 and 24: Applicant has amended the claims to clarify that they refer to the ground power source of claim 6.

Claim 19: The Examiner asserts that the limitation "a drain terminal connected to one of the level conversion outputs" in line 8 is incorrect. Applicant disagrees; however, the claim has been amended to be more clear. An example of claim 19 is shown in figure 33. In this figure there are two level conversion outputs (OUTH, OUTB) and there are at least two p-MOSs whose gate terminals are connected to the control circuit (C0, C1). Each of the drains of these two p-MOSs are connected to either OUTH or OUTB. There are at least two additional p-MOSs whose gate terminals are connected to the third logic circuit (E1). Each of the drains of these two p-MOSs are connected to either OUTH or OUTB.

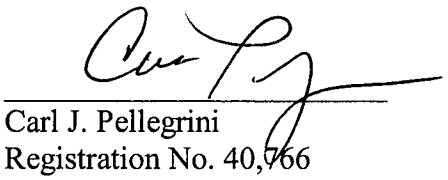
Claims 22 and 24: The Examiner asserts that the limitation "level shift outputs" is incorrect. Applicant has amended the claims to clarify them.

Claim 68: The Examiner asserts that the limitation "a level conversion output" in line 11 is unclear as to if this level conversion output is different from the level conversion output signal recited in lines 5-6. Applicant has amended the claim to clarify it.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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